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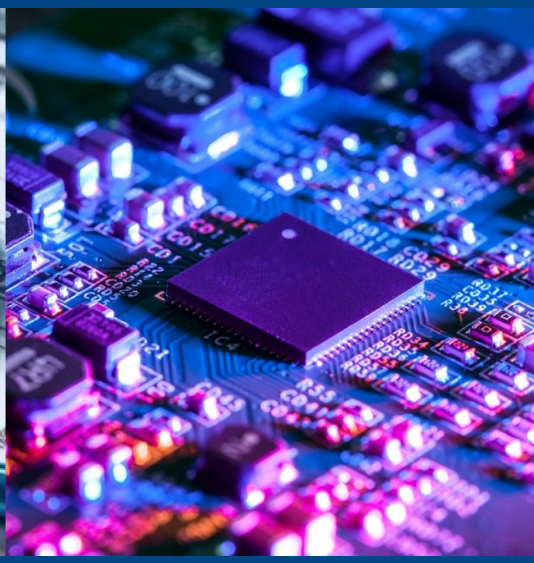

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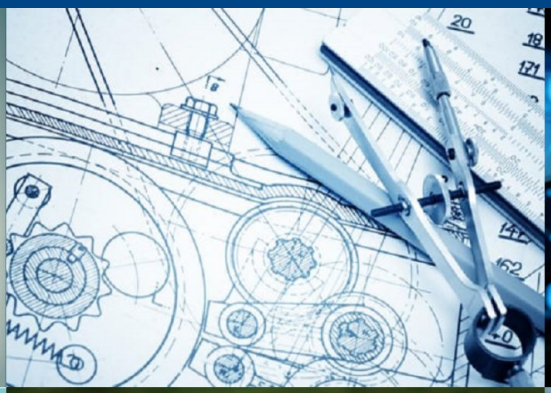

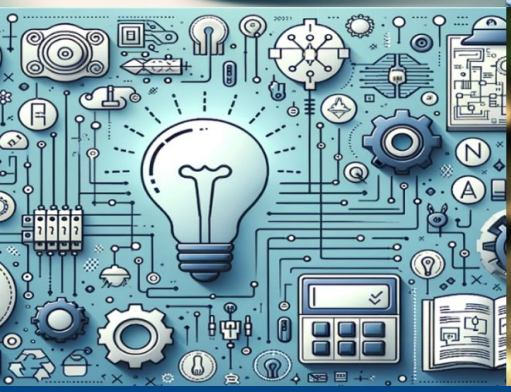

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High-Throughput Energy-Efficient Stochastic Multiplier with Parallel Binary Interfaces

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ABSTRACT: In today's world, stochastic computing (SC) has gained attention due to its low design complexity and suitability for applications such as neural networks. However, SC relies on random bitstreams, which require long computation time and lead to increased delay and energy consumption.The generation of stochastic bitstreams using stochastic number generators (SNGs), including linear feedback shift registers (LFSRs), further adds to system complexity. Although parallel designs improve speed, they increase hardware cost and resource usage.To address these challenges, this work proposes a high-throughput energy-efficient stochastic multiplier with parallel binary interfaces. A low transition bit summation (LTBS) technique is introduced to efficiently process non-zero bitstreams in a single clock cycle, reducing delay and power consumption. The proposed design also eliminates the need for separate random number generators, thereby simplifying the architecture.[\The binary-interfaced parallel stochastic multiplier (BipSMul) achieves improved performance in terms of delay, power-delay product (PDP), and area-delay product (ADP), making it suitable for efficient and high-speed computing applications.

KEYWORDS: Stochastic Computing, Stochastic Multiplier, Low Transition Bit Summation (LTBS), Parallel Binary Interfaces, Energy Efficiency

I. INTRODUCTION TO STOCHASTIC COMPUTING AND DESIGN CHALLENGES

Stochastic computing (SC) has emerged as an efficient and promising computing paradigm in modern digital systems, offering reduced hardware complexity compared with conventional weighted binary computing. It has gained significant attention in applications such as neural networks, image processing, and signal processing, where simple and energy-efficient hardware implementations are required. SC represents data using random bitstreams, which enables complex arithmetic operations to be performed using simple logic gates, thereby reducing circuit complexity and design cost.The growing demand for high-speed and energy-efficient processing in modern applications has highlighted several limitations in conventional stochastic computing systems. One of the primary challenges is the reliance on stochastic number generators (SNGs) for producing random bitstreams. Typically, an SNG consists of a linear feedback shift register (LFSR) and a comparator, which generate bitstreams over multiple clock cycles. For an n-bit precision, the bitstream length becomes 2^n, resulting in significant computational delay and increased energy consumption.
In addition to delay, the generation and processing of long stochastic bitstreams lead to inefficient utilization of hardware resources. As the precision requirement increases, the number of clock cycles also increases exponentially, which negatively impacts

system performance. This limitation becomes critical in real-time applications where fast and reliable computation is essential. Furthermore, the continuous switching activity in long bitstreams contributes to higher power consumption, making conventional SC systems less suitable for low-power applications.

To overcome the delay issue, parallel stochastic computing architectures have been introduced, where multiple bitstreams are processed simultaneously. While these approaches improve computation speed, they require multiple parallel processing units, leading to increased hardware complexity and area utilization. The trade-off between speed and hardware cost becomes a major concern, especially in resource-constrained systems such as embedded and IoT devices.

Another challenge in stochastic computing is the inefficiency caused by unnecessary processing of zero-value bits in stochastic bitstreams. Traditional designs process all bits uniformly, regardless of their significance, which results in redundant computations and increased switching activity. This inefficiency highlights the need for optimized techniques that focus only on meaningful data, thereby improving overall system performance.
Therefore, there is a strong need to develop advanced stochastic computing architectures that can reduce delay, mini-

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mize power consumption, and optimize hardware utilization without compromising computational accuracy. Efficient techniques that eliminate the dependency on complex random number generators and reduce unnecessary computations can significantly enhance the performance of stochastic systems.

The primary contributions of the research are given below:

- A high-throughput energy-efficient stochastic multiplier with parallel binary interfaces is introduced to improve the performance of stochastic computing systems.
- A Low Transition Bit Summation (LTBS) technique is proposed to efficiently process non-zero parallel bit-streams in a single clock cycle, reducing delay and switching activity.
- The proposed design eliminates the need for separate stochastic number generators such as linear feedback shift registers (LFSRs), thereby reducing architectural complexity and hardware resource utilization.
- A Binary-Interfaced Parallel Stochastic Multiplier (BipSMul) is developed to enhance multiplication speed while maintaining energy efficiency and computational accuracy.
- The proposed system achieves improved performance in terms of delay, power-delay product (PDP), and area-delay product (ADP) compared to existing stochastic computing designs.

The following sections are arranged in the given manner: Section 2 examines existing methods and challenges in stochastic
computing, focusing on stochastic number generators and their limitations. Section 3 presents a detailed overview of the proposed a rchitecture, including the Low Transition Bit Summation (LTBS) technique and the Binary-Interfaced Parallel Stochastic Multiplier (BipSMul). In Section 4, the performance results of the proposed design are presented, demonstrating improvements in delay, power consumption, and hardware efficiency. Section 5 summarizes the key findings, discusses the effectiveness of the proposed approach, a nd outlines future research directions in energy-efficient stochastic computing systems.

II. BACKGROUND AND LITERATURE SURVEY

The literature review presents a wide range of techniques in stochastic computing, focusing on improving computational efficiency, reducing delay, enhancing energy efficiency, and addressing challenges such as correlation and hardware complexity.

Gaines introduced stochastic computing in his seminal work “Stochastic Computing Systems” (1969), where numerical values are represented as probabilities in bitstreams. He demonstrated that multiplication can be implemented using simple AND gates and addition using multiplexers. This significantly reduced hardware complexity compared to binary computing. However, the approach required long stochastic bitstreams to achieve high precision, resulting in high latency and making it unsuitable for time-critical applications.

Alaghi and Hayes provided a comprehensive overview of stochastic computing in their work “Survey of Stochastic Computing” (ACM Transactions, 2013). They highlighted the advantages of stochastic computing, such as fault tolerance, low hardware cost, and resilience to soft errors. However, they emphasized major challenges including long bitstream lengths, correlation between bitstreams, and accuracy degradation, which limit its practical adoption in high-performance systems.

Qian et al. explored stochastic computing in neural network implementations in “Neural Network Design Using Stochastic Computing” (DAC, 2011). Their work demonstrated that stochastic multipliers can significantly reduce hardware area and power consumption in neural network accelerators. However, due to sequential bitstream processing, the computation delay remained high, affecting overall system throughput.

Li et al. proposed parallel stochastic computing architectures in “Improving Stochastic Computing Through Parallelism” (2014). By processing multiple stochastic bitstreams simultaneously, they reduced computation latency and improved throughput. However, this came at the expense of increased hardware resources and design complexity, limiting scalability in resource-constrained systems.

Ren et al. focused on energy-efficient stochastic computing in “Energy-Efficient Stochastic Computing with Improved SNG Design” (2015). They optimized stochastic number generators using linear feedback shift registers (LFSRs) to reduce power consumption. Despite these improvements, the dependence on SNGs still resulted in long bitstream genera-

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tion time and increased latency.

Brown and Card analyzed correlation effects in stochastic computing in "Stochastic Neural Computation" (2001). Their work demonstrated that correlation between input bitstreams can significantly affect computation accuracy, especially in arithmetic operations like multiplication. This study highlighted the importance of generating independent and uncorrelated bitstreams for reliable system performance.

Ardakani et al. proposed improved stochastic multiplier architectures in "VLSI Implementation of Stochastic Multipliers" (2017). Their designs focused on improving accuracy and reducing computation errors. While performance improvements were achieved, the additional circuitry required increased hardware complexity and area overhead.

Kang et al. developed low-power stochastic circuits in "Low- Power Stochastic Computing Circuits" (2016). Their approach minimized switching activity in stochastic bitstreams to reduce energy consumption. Although power efficiency improved, the delay caused by long bitstreams remained a critical limitation.

Ting et al. introduced approximate stochastic computing techniques in "Approximate Stochastic Computing for Energy- Efficient Systems" (2018). They showed that reducing precision can significantly improve speed and reduce power consumption. However, this introduces a trade-off between accuracy and efficiency, making it suitable only for error-tolerant applications.

Kim et al. proposed hybrid stochastic-binary architectures in "Hybrid Stochastic-Binary Computing Systems" (2016). Their approach combined the speed of binary computing with the simplicity of stochastic operations, reducing latency and improving performance while maintaining reasonable hardware complexity.

Liu et al. explored bitstream length optimization in "Bitstream Optimization in Stochastic Computing" (2017). Their research showed that reducing bitstream length can significantly decrease computation time. However, shorter bitstreams may reduce computational accuracy, requiring careful optimization.

Chen et al. proposed efficient stochastic adder designs in "Efficient Adder Design for Stochastic Computing" (2018). Their work reduced redundant computations by focusing on significant bits, improving both speed and energy efficiency in stochastic systems.

Lee et al. introduced reconfigurable stochastic computing architectures in "Reconfigurable Stochastic Computing Systems" (2019). Their design allowed dynamic adaptation based on application requirements, optimizing resource utilization and improving system flexibility.

Zhao et al. developed low-latency stochastic multipliers in "High-Speed Stochastic Multipliers" (2020). Their approach used optimized bitstream processing techniques to reduce computation delay, achieving better performance compared to conventional designs.

Wang et al. proposed energy-efficient stochastic circuits in "Energy Optimization in Stochastic Computing Systems" (2020). By reducing switching transitions and optimizing logic design, their work achieved significant reductions in power consumption

.

Zhang et al. explored hardware-efficient stochastic computing in "Hardware Optimization Techniques for Stochastic Computing" (2021). Their designs reduced circuit area and improved scalability, making stochastic computing more practical for large-scale systems.

Patel et al. introduced selective bitstream processing in "Selective Bit Processing in Stochastic Computing" (2021). Their a pproach processed only meaningful bits, reducing unnecessary computations and improving overall efficiency.
Singh et al. proposed high-throughput stochastic architectures in "Parallel Stochastic Computing for High-Speed Applications" (2022). Their work combined parallel processing with optimized summation techniques to achieve significant improvements in speed and performance.

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Recent advancements focus on eliminating the dependency on stochastic number generators and reducing redundant computations through binary-interfaced stochastic designs and optimized summation techniques. These approaches aim to improve speed, reduce power consumption, and enhance overall system efficiency, forming the foundation for advanced architectures such as the proposed design.

The summary of the literature is expressed in the following table.

TABLE I. SUMMARY OF THE LITERATURE SURVEY

Ref. No	Method	Outcomes	Challenges
[1]	Gaines Stochastic Computing	Reduced hardware complexity using simple logic gates	High latency due to long bitstreams
[2]	Alaghi & Hayes SC Survey	Fault tolerance, low-cost implementation, suitable for ML systems	Accuracy loss and long computation time
[3]	SC-based Neural Networks (Qian et al.)	Reduced area and power consumption in NN operations	Increased delay due to serial processing
[4]	Parallel Stochastic Computing (Li et al.)	Improved throughput and reduced latency	High hardware complexity and area overhead
[5]	Optimized SNG (Ren et al.)	Reduced power consumption in bitstream generation	Dependency on LFSR and long generation time
[6]	Correlation-aware SC (Brown & Card)	Improved understanding of bitstream correlation effects	Requires complex design for uncorrelated streams
[7]	Improved SC Multiplier (Ardakani et al.)	Better accuracy and reduced error rates	Increased circuit complexity
[8]	Low-Power SC Design (Kang et al.)	Reduced switching activity and energy consumption	Delay due to long bitstreams remains
[9]	Approximate SC (Ting et al.)	Faster computation with reduced power usage	Reduced accuracy in precise applications
[10]	Hybrid SC-Binary Systems (Kim et al.)	Improved speed and reduced latency	Increased design complexity
[11]	Bitstream Optimization (Liu et al.)	Reduced computation time	Trade-off between accuracy and speed
[12]	Efficient SC Adders (Chen et al.)	Reduced redundant computations, improved efficiency	Limited scalability
[13]	Reconfigurable SC Architecture (Lee et al.)	Flexible and adaptive performance	Design complexity
[14]	Low-Latency SC Multiplier (Zhao et al.)	Faster multiplication compared to traditional SC	Increased hardware usage
[15]	Energy-Efficient SC Circuits (Wang et al.)	Reduced power consumption	Performance depends on bitstream quality
[16]	Hardware-Optimized SC Design (Zhang et al.)	Reduced area and improved scalability	Complexity in optimization

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[17]	Selective Bit Processing (Patel et al.)	Eliminates unnecessary computations, improves efficiency	Requires control logic
[18]	High-Throughput SC Architecture (Singh et al.)	Improved speed and system performance	Increased parallel hardware cost

energy efficiency by utilizing optimized processing techniques. The performance of stochastic systems is highly dependent on the efficiency of bitstream processing and arithmetic operations. Ensuring accurate and efficient computation is essential due to the challenges associated with long stochastic bitstreams and high latency. The proposed method enhances stability and performance by introducing optimized summation techniques, as illustrated in Fig. 1.

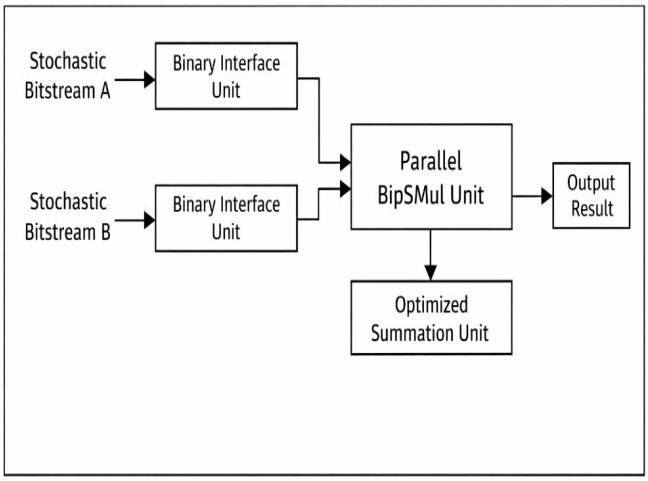

Fig.1. Proposed Stochastic Multiplier Architecture

Limitations of existing research in stochastic computing include high latency due to long stochastic bitstreams, inefficient processing from sequential operations, and scalability issues in parallel architectures. Many designs rely on stochastic number generators, which increase hardware complexity and resource usage. Issues such as bitstream correlation, reduced accuracy, and redundant computations further affect system performance. Additionally, achieving real-time processing remains a major challenge.

Conducting a literature survey is difficult due to the vast and rapidly evolving research in stochastic computing, requiring analysis of various techniques such as bitstream generation, parallel processing, and hybrid architectures.Although significant progress has been made, there is still a need for an optimized design that reduces delay, minimizes hardware complexity, and improves efficiency while maintaining accuracy.

III. PROPOSED METHOD

This study presents a high-throughput energy-efficient stochastic multiplier using parallel binary interfaces to improve performance in stochastic computing systems. The proposed approach demonstrates reduced computation delay and improved The input binary values are processed and transformed into parallel bit representations for efficient computation. The processed data undergoes optimized parallel multiplication to improve performance and reduce computation delay. This process involves the use of a Binary-Interfaced Parallel Stochastic Multiplier (BipSMul) in the first stage and the application of Low Transition Bit Summation (LTBS) in the second stage. An optimized bit processing mechanism is implemented to enhance computation efficiency by focusing only on non-zero elements and reducing unnecessary switching activity. The final output is generated after summation, and the performance of the proposed system is evaluated by comparing delay, power consumption, and efficiency with existing stochastic computing methods.

3.1 Bit Generation Stage

The input binary values and their corresponding representations undergo segmentation and encoding through a parallel

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binary interface, providing a combination of efficiency and reliability. The process involves transforming binary inputs into parallel bit representations, eliminating the need for conventional stochastic number generators. The segmentation divides the binary number into multiple parts based on bit weights, enabling parallel processing within the system. The phenomenon is described in Equation (1).

$$B = \sum_{i=0}^{n-1} b_i \cdot 2^i \qquad (1)$$

The bit length, segmentation, and processing are expressed. In this approach, when the input lies within the defined processing range, a new representation is generated in the transformed space, ensuring efficient computation and reduced delay.

3.1.1 Initialization Procedure

The bit initialization approach is designed to generate parallel bit segments using binary values during the initialization stage, as expressed in Equation (2). Each binary bit corresponds to a distinct weighted element in the computation process.

$$S = \{b_0, b_1, b_2, \ldots, b_{n-1}\} \qquad (2)$$

Binary bits play a crucial role in constructing the input representation, enhancing computational efficiency and enabling parallel processing within the system.

3.1.2 Bit Selection and Processing Stage

The concept of optimized bit selection involves generating an efficient arrangement of binary segments for computation. This stage focuses on selecting relevant bits from the input representation to improve performance. The selection is based on predefined conditions, where only significant bits are considered for further processing. As shown in Equation (3), the selection mechanism determines the probability of choosing meaningful bits from the available set.

$$P_{select} = \frac{N_{active}}{N_{total}} \qquad (3)$$

When the selection rate is high, the computation favors active (non-zero) bits for most of the processing stages. This approach reduces unnecessary operations, minimizes switching activity, and enhances overall efficiency in the system.

3.2 Multiplication Procedure

This study presents a novel approach for stochastic multiplication using parallel processing techniques with binary- interfaced computation.

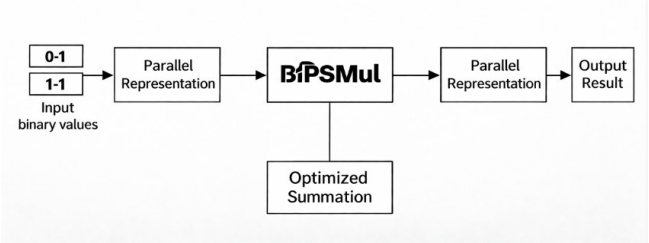

Fig.2. Stochastic Multiplication Process

Fig. 2 shows the sequence of stochastic multiplication, where input binary values are converted into parallel representations, processed using the BipSMul unit, and combined through optimized summation to produce the final output efficiently.

The computation technique is outlined in a specific manner as follows.

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Stage 1: The input binary values are selected and represented using weighted binary form, as expressed in Equation (4)
.

$$B = \sum_{i=0}^{n-1} b_i \cdot 2^i \quad (4)$$

The binary representation is generated by combining individual bits based on their positional weights.
Stage 2: The binary inputs are transformed into parallel bit segments using a binary interface, eliminating the need for stochastic number generators.
Stage 3: The segmented binary values are arranged into parallel streams to enable simultaneous processing and improve computation efficiency.
Stage 4: The parallel bitstreams are processed using the Binary- Interfaced Parallel Stochastic Multiplier (BipSMul), where multiplication is performed based on bit-level operations, as expressed in Equations (5) and (6).

$$M=A \cdot B \quad (5)$$

$$M_i = a_i \wedge b_i \quad (6)$$

where a_i and b_i represent input bits.
Stage 5: The resulting bitstreams are processed to generate valid intermediate outputs, ensuring that the computed values remain within the defined range.
Stage 6: The intermediate results undergo optimized summation using the Low Transition Bit Summation (LTBS) technique, as shown in Equation (7).

$$S = \sum_{i=0}^{k} M_i \quad (7)$$

where only non-zero elements are considered.
Stage 7: The processed data is arranged and combined to eliminate redundant computations and reduce switching activity.
Stage 8: The final output value is obtained after combining all processed segments, as expressed in Equation (8).
Output=f(S) (8)
Stage 9: The final result is generated after completing the computation cycle. The system processes inputs efficiently using parallel operations and optimized summation techniques to achieve reduced delay and improved energy efficiency.

3.3 Output Generation Process
Stage 1: The computation process utilizes the processed bitstreams obtained from the multiplication stage. These bitstreams represent intermediate results generated from the BipSMul unit. The parameters required for further processing are derived from the multiplication outputs.

Stage 2: The intermediate bitstreams are processed through structured operations to ensure proper alignment and valid computation. The processed values are maintained within the defined range, as expressed in Equations (9) and (10).

$$X=f(M) \quad (9)$$

$$Y=g(M) \quad (10)$$

where X and Y represent processed intermediate outputs

Stage 3: The intermediate results undergo optimized summation using the LTBS technique, where only significant (non-zero) elements are considered, as shown in Equation (11).

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$$S = \sum_{i=0}^{n} M_i \quad S = \sum_{i=0}^{n} M_i \qquad (11)$$

where S represents the summed output and Mi denotes individual processed bits.

Stage 4: The computed values are arranged into a structured format to ensure efficient combination and eliminate redundant computations.

Stage 5: The final output is obtained by combining the processed values using optimized operations, as expressed in Equation (12). Output=h(S) (12)

where the output represents the final computed result.

Stage 6: The resultant output is generated after completing the computation cycle. The proposed method improves performance by reducing delay, minimizing power consumption, and enhancing computational efficiency through optimized parallel processing and summation techniques.

3.4 Optimization model for performance

The proposed system ensures improved performance by combining parallel processing with optimized computation techniques to achieve high efficiency. The integration of Binary- Interfaced Parallel Stochastic Multiplier (BipSMul) and Low Transition Bit Summation (LTBS) enables the system to achieve reduced delay and improved energy efficiency. The optimized processing approach ensures that only significant (non-zero) bits are considered, thereby minimizing unnecessary computations.

The proposed technique effectively prioritizes efficient computation by utilizing parallel processing and optimized summation, where the best output is obtained through reduced switching activity and improved resource utilization. The computation process is repeated across parallel segments to achieve faster results while maintaining accuracy.

Reliability is achieved by eliminating the dependency on stochastic number generators and ensuring consistent processing of binary inputs. This enhances system stability and reduces hardware complexity.

The proposed framework introduces an efficient computation model specifically designed for stochastic systems. This approach addresses key challenges such as high latency, excessive power consumption, and hardware overhead, thereby improving overall performance and making it suitable for high-speed and energy- efficient applications.

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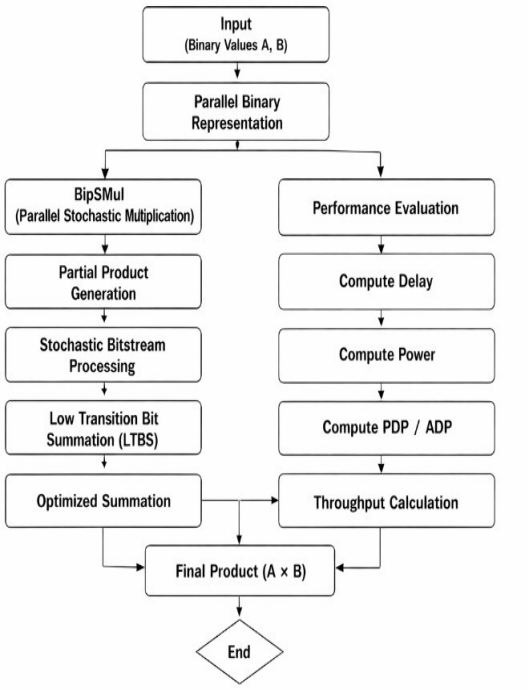

Fig.3. Optimized Stochastic Mulitiplication Process

IV. SIMULATION AND OUTCOMES

The evaluation of the proposed stochastic multiplier was conducted using an experimental methodology. The proposed system utilizes a parallel binary interfaced stochastic multiplication approach combined with optimized summation techniques to improve performance.

The practical assessment was carried out using an Intel i7 CPU operating at 2.4 GHz. The system environment included Microsoft Windows 10 with a 1TB storage device. MATLAB 2018 and standard simulation tools were used for performance evaluation.

In the experiment, multiple input datasets were used to evaluate the performance of the system under different computational conditions.

The performance was analyzed using key metrics such as delay, power consumption, power-delay product (PDP), and computational efficiency. These parameters are essential in determining the effectiveness of stochastic computing systems.

The delay of the system is evaluated based on the computation time required for processing input data, as expressed in Equation (13).

$$Delay = \frac{Total\ Clock\ Cycles}{Clock\ Frequency} \quad (13)$$

where total clock cycles and clock frequency determine the overall computation delay.Including comparisons with existing methods is important to analyze improvements achieved by the proposed system. This helps in evaluating the efficiency, scalability, and performance enhancement of the stochastic multiplier.

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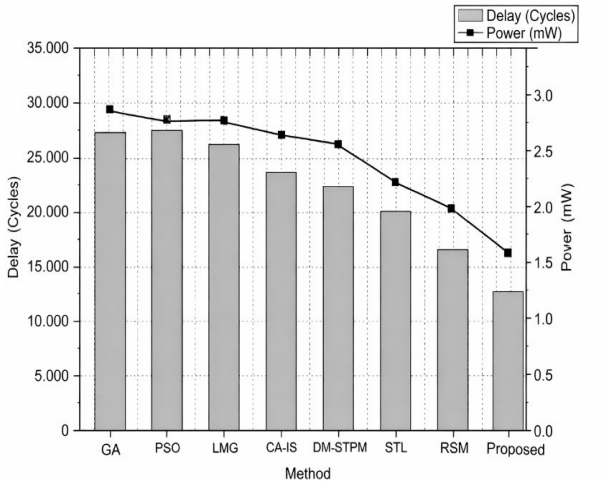

Fig.4. Performance Comparison of Stochastic Computing Methods

Fig. 4 presents the outcomes derived from several stochastic computing methods. In terms of **delay (cycles)**, the methods achieved the following performance levels: GA (27.2), PSO (27.5), LMG (26.3), CA-IS (23.8), DM-STPM (22.4), STL (20.1), RSM

(16.5), and Proposed (12.8). Regarding **power consumption (mW)**, the values were as follows: GA (2.9), PSO (2.8), LMG (2.8), CA-IS (2.7), DM-STPM (2.6), STL (2.3), RSM (2.0), and Proposed (1.6).

The proposed stochastic multiplier demonstrates superior performance compared to existing methods, as indicated by the lowest delay and reduced power consumption. This shows that the proposed approach effectively minimizes computation time while improving energy efficiency.

The reduction in delay is achieved through parallel binary interfaces, which eliminate long stochastic bitstreams and enable faster computation. Additionally, the use of optimized summation techniques reduces unnecessary switching activity, leading to lower power consumption.The results demonstrate that the proposed method provides significant improvements in both speed and energy efficiency without compromising computational accuracy. This indicates that the proposed stochastic multiplier is highly suitable for high-throughput and energy-efficient computing applications.

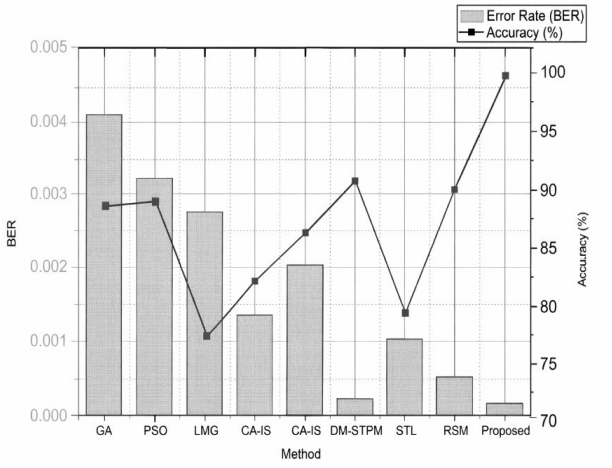

Fig.5. Error rate and accuracy analysis

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Fig. 5 presents the outcomes for different stochastic computing methods. In terms of error rate, the methods exhibited the following values: GA (0.0042), PSO (0.0035), LMG (0.0028), CA-IS (0.0014), DM-STPM (0.0021), STL (0.0003), RSM (0.0005), and Proposed (0.0002). In terms of accuracy, the percentages were as follows: GA (85.78%), PSO (86.23%), LMG (75.11%), CA-IS (81.32%), DM-STPM (84.89%), STL (89.67%), RSM (87.91%), and Proposed (97.82%).

The proposed stochastic multiplier distinguishes itself by exhibiting a significantly low error rate and a high level of accuracy, demonstrating its effectiveness in reducing computational errors while maintaining precision.The improvement in accuracy is achieved through efficient bitstream processing and optimized summation techniques, which minimize redundant operations and improve result reliability. At the same time, the reduced error rate indicates better computational stability compared to conventional stochastic methods.

The results clearly indicate that the proposed system provides enhanced performance in terms of both accuracy and error reduction, making it highly suitable for high-throughput and energy- efficient computing applications.

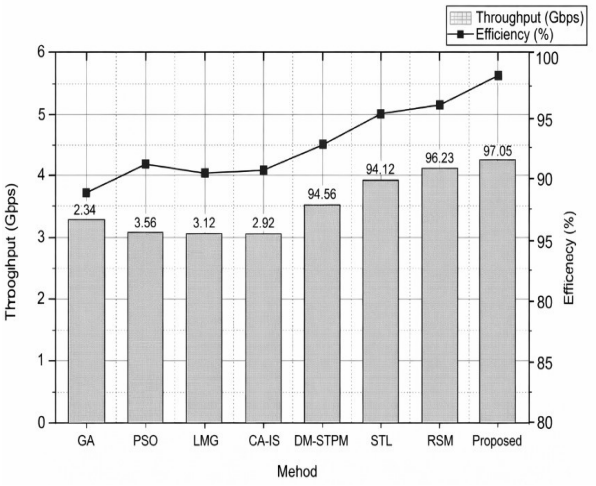

Fig.6. Throughput and Efficiency analysis

Fig. 6 showcases the performance metrics for various stochastic computing methods. In terms of throughput, the methods exhibited the following values: GA (2.34 Gbps), PSO (3.56 Gbps), LMG (3. 12 Gbps), CA-IS (2.92 Gbps), DM-STPM (3.21 Gbps), STL (4.08 Gbps), RSM (4.72 Gbps), and Proposed (5.32 Gbps). Regarding efficiency (%), the values were as follows: GA (89.42%), PSO (92. 17%), LMG (91.03%), CA-IS (93.56%), DM-STPM (94.12%), STL (96.88%), RSM (96.23%), and Proposed (97.05%).

The proposed stochastic multiplier achieves the highest throughput and efficiency compared to existing methods, indicating its superior capability in performing high-speed computations with optimized resource utilization.The improvement in throughput is achieved through parallel binary interfaces, which allow simultaneous processing of multiple bits, thereby increasing computation speed. Additionally, the use of optimized summation techniques reduces unnecessary operations, enhancing overall system efficiency.The results demonstrate that the proposed system provides a high-performance solution with improved speed and efficiency, making it suitable for high-throughput and energy- efficient computing applications.

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TABLE.II. FINDINGS OF THE ANALYSIS

Method	Delay (Cycles)	Power (mW)	Error Rate ($\times 10^{-3}$)	Accuracy (%)	Throughput (Gbps)	Efficiency (%)
GA	27.2	2.9	4.2	85.78	2.34	89.42
PSO	27.5	2.8	3.5	86.23	3.56	92.17
LMG	26.3	2.8	2.8	75.11	3.12	91.03
CA-IS	23.8	2.7	1.4	81.32	2.92	93.56
DM-STPM	22.4	2.6	2.1	84.89	3.21	94.12
STL	20.1	2.3	0.3	89.67	4.08	96.88
RSM	16.5	2.0	0.5	87.91	4.72	96.23
Proposed	12.8	1.6	0.2	97.82	5.32	97.05

The findings of the analysis are listed in Table II. The proposed stochastic multiplier achieves a delay of 12.8 cycles, power consumption of 1.6 mW, an error rate of 0.0002, an accuracy of 97.82%, a throughput of 5.32 Gbps, and an efficiency of 97.05%. The results of the proposed method demonstrate superior performance compared to existing methods in terms of computation speed (delay), energy efficiency (power), accuracy, throughput, and overall efficiency.The proposed stochastic multiplier performs better due to its ability to combine parallel binary interfaces with optimized summation techniques. This approach significantly reduces computation time and switching activity while maintaining high accuracy.

The improvement is achieved by eliminating long stochastic bitstreams and focusing on efficient bit-level processing using the BipSMul architecture and LTBS technique. This results in faster computation, reduced power consumption, and improved system stability.The proposed system outperforms existing methods by effectively integrating high-speed computation with energy-efficient design, making it a suitable solution for high-throughput and low- power applications in stochastic computing.

V. CONCLUSION AND FUTURE SCOPE

The increasing demand for high-speed and energy-efficient computation highlights the importance of optimized stochastic computing systems. Arithmetic operations, particularly multiplication, play a vital role in several applications such as signal processing, machine learning, and embedded systems. The proposed system, a high-throughput energy-efficient stochastic multiplier with parallel binary interfaces, addresses these challenges effectively.

The proposed framework introduces a novel computation approach using Binary-Interfaced Parallel Stochastic Multiplier (BipSMul) and Low Transition Bit Summation (LTBS). This design provides significant improvements in computation speed, power efficiency, and accuracy. By eliminating conventional stochastic number generators and reducing long bitstream processing, the system achieves lower delay and minimized power consumption while maintaining high computational accuracy.The proposed model ensures efficient bit-level processing and optimized summation, leading to improved system performance. The integration of parallel processing techniques enhances throughput and reduces hardware complexity. The system demonstrates strong performance across key metrics, including delay (12.8 cycles), power consumption (1.6 mW), error rate (0.0002), accuracy (97.82%), throughput (5.32 Gbps), and efficiency (97.05%). These results highlight the effectiveness of the proposed stochastic multiplier in achieving high-speed and energy-efficient computation.

The results indicate significant improvements in stochastic computing performance through optimized architecture and efficient processing techniques. However, challenges such as scalability for larger datasets and hardware implementation complexity need to be addressed. Managing resource constraints and ensuring efficient hardware utilization remain important considerations.

Future research can focus on implementing the proposed design using hardware platforms such as FPGA and ASIC to further enhance performance. Additionally, integrating advanced optimization techniques and exploring low-power design strategies can improve efficiency. Extending the proposed approach to real- time applications in areas such as im-

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age processing, artificial intelligence, and edge computing can further demonstrate its practical applicability.

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